UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/722,404	11/28/2000	Hidekazu Takata	3917-2	4573

23117 7590 02/10/2005

NIXON & VANDERHYE, PC
1100 N GLEBE ROAD
8TH FLOOR
ARLINGTON, VA 22201-4714

EXAMINER	
ABRISHAMKAR, KAVEH	
ART UNIT	**PAPER NUMBER**
2131	

DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/722,404	TAKATA ET AL.	
	Examiner	Art Unit	
	Kaveh Abrishamkar	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/21/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This action is in response to the amendment filed on September 27, 2004. Claims 1 – 18 were originally received for consideration. Per the received amendment, claims 1 – 18 are amended, and claims 19-32 are newly added. Claims 1 – 32 are currently being considered.

Information Disclosure Statement

2. An initialed and dated copy of the Applicant's IDS form 1449, received March 21, 2001, is attached to this Office action.

Response to Arguments

3. Applicant's arguments, filed on September 27, 2004, have been fully considered but they are not persuasive because of the following reasons:

Regarding amended independent claims 1,7,8,9,14, and newly added independent claims 19 and 28, the applicant argues that the cited prior art (CPA), Takata (U.S. Patent No. 6,594,777), does not teach the newly added limitation "the second portion of the regular data being necessary for use of the regular data." The applicant further argues that the claimed "dummy data" is not

analogous in nature to the "defective" memory cells disclosed in the CPA. These arguments are not considered persuasive. As stated in the previous Office action, the "dummy data" is interpreted as data which has "no useful information" and therefore, is analogous in nature to the "defective" data disclosed in the CPA, as both are not useful for the running of the program unless replaced by another data, referred to as the "second portion" in the application, and referred to as "modified data" in the CPA. Furthermore, the memory region being replaced ***do not*** have to be only for "defective" memory cells, but can be for replacing data with updated modified data (column 2 lines 30-42), which is analogous to updating dummy data with the second portion data. Regarding the applicant's assertion that the CPA fails to teach "the second portion of the regular data being necessary for use of the regular data," the CPA does disclose this limitation through its diagrams and preferred embodiments. The CPA discloses that the modified data or the defective data (dummy data) which is updated with the new modified data occurs within the same memory block (program) (Figure 7, block 1). Furthermore, the preferred embodiments include a video game machine, which is well-known to be a program in which each memory block which would need to be updated (with modified data) is needed to run the program in its entirety. Regarding dependent claims 4 and 12, applicant claims that the CPA does not teach or suggest, "different writing voltages are used for different portions of the semiconductor nonvolatile memory." This argument is not found persuasive. In multi-value masked ROMs as disclosed by the applicant and the CPA, it is well-known that different potential levels are provided

for read-out of data from a selected memory cell, these different potential levels corresponding to the multi-value data stored in the memory cells. In these situations, the multi-value data have been written into each memory cell (Figure 7) by supplying different levels of writing voltage based on the multi-value data to be stored. This allows the stored multi-value data to be read-out by specifying the respective voltage levels with which the data have been written. Therefore the obviousness rejection for these claims is respectfully maintained. Accordingly, the rejection for the original claims 1 – 18 is maintained, and the rejection is applied to the new claims 19-32, which are analogous to the rejected claims, but provide for a video game program, which is a preferred embodiment of the cited prior art, Takata.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 – 18 are rejected under 35 U.S.C. 103(a) as being obvious over Takata (U.S. Patent 6,594,777).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it

constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2). The application being examined deals with a semiconductor storage device with a first store which stores regular data and a dummy data portion, and has a second store which stores the second portion of the regular data to be originally stored in the dummy data portion. The previous application, now U.S. Patent 6,594,777, has a first store that stores regular data but has defective data, which can be replaced with data from the second store that holds a modification data. It would have been obvious to use the dummy data instead of the defective data

since both have no useful information, and replace it with a regular data instead of the modification data, to complete the data block.

Regarding claim 1, Takata discloses:

A semiconductor memory device storing regular data and having a security function for preventing unauthorized use of the regular data (column 1 lines 36 – 52), comprising:

a first store including a first storing area for fixedly storing a first portion of the regular data and a dummy data storing area for fixedly storing dummy data in place of a second portion of the regular data, the second portion of the regular data being necessary for use of the regular data; (column 3 lines 45 – 63);

a second store including a second storing area which has a storage capacity equal to at least a storage capacity of the dummy data storing area of the fist store and fixedly stores the second portion of the regular data (Figure 1 item 21B, column 3 lines 40 – 63); and

a read control circuit which compares an input address with a dummy address corresponding to an address space of the dummy data storing area, and which enables reading of the first portion of the regular data from the first store when the input address and the dummy address do not correspond, and disables the reading of the first portion of the regular data and enables the reading of the second portion of the regular data from the second store when the input address and the dummy address correspond (Figure 1 item 21A, column 2 lines 31 – 42, column 5 lines 3 – 21).

Takata does not explicitly disclose the presence of a dummy data in a first storing region. Takata describes the presence of defective data in the first storing area (column 3 lines 45 – 63). The defective data is analogous to the dummy data delineated in the application in that both kinds of data do not serve contain information necessary for the proper utilization of the data block, and both data types need to be replaced with useful data. The defective data is replaced with modification data, which is analogous to the dummy data being replaced with regular data. Both functions result in the completion of a data block by replacing one non-regular data with the regular data. Therefore it would have been obvious at the time the applicant's invention was made to use dummy data instead of the defective data because both are same in function and both are replaced with a regular data to complete the data block. This replacement of the defective or dummy data would provide a benefit in adding or modifying of an "unwritable memory device used in game machines, mobile terminals, and the like" (column 1 lines 5 – 10).

Regarding claim 7, Takata discloses:

A memory device storing an application program and having a security function for preventing unauthorized use of the application program, comprising:

a first store including a first program storing area for fixedly storing a first portion of the application program and a dummy data in place of a second portion of the application program, the second portion of the application program being necessary for use of the application (column 3 lines 45 – 63);

a second store including a second program storing area which has a storage capacity equal to at least a storage capacity of the dummy data storing area of the first store and fixedly stores the second portion of the application program (Figure 1 item 21B, column 3 lines 40 – 63); and

a read control circuit which compares an input address with a dummy address corresponding to an address space of the dummy data storing area, and which enables reading of the first portion of the application program from the first store when the input address and the dummy address do not correspond and disables the reading of the first portion of the application program and enables the reading of the second portion of the application program from the second store when the input address and the dummy address correspond (Figure 1 item 21A, column 2 lines 31 – 42, column 5 lines 3 – 21).

Takata does not explicitly disclose the presence of a dummy data in a first storing region. Takata describes the presence of defective data in the first storing area (column 3 lines 45 – 63). The defective data is analogous to the dummy data delineated in the application in that both kinds of data do not serve contain information necessary for the proper utilization of the data block, and both data types need to be replaced with useful data. The defective data is replaced with modification data, which is analogous to the dummy data being replaced with regular data. Both functions result in the completion of a data block by replacing one non-regular data with the regular data. Therefore it would have been obvious at the time the applicant's invention was made to use dummy data instead of the defective data because both are same in function and both

are replaced with a regular data to complete the data block. This replacement of the defective or dummy data would provide a benefit in adding or modifying of an "unwritable memory device used in game machines, mobile terminals, and the like" (column 1 lines 5 – 10).

Regarding claim 8, Takata discloses:

An electronic device for storing an application program and having a security function for preventing unauthorized use of the application program, comprising:

a first store including a first program storing area for fixedly storing a first portion of the application program and a dummy data in place of a second portion of the application program, the second portion being necessary for the use of the application program (column 3 lines 45 – 63);

a second store including a second program storing area which has a storage capacity equal to at least a storage capacity of the dummy data storing area of the first store and fixedly stores the second portion of the application program (Figure 1 item 21B, column 3 lines 40 – 63); and

a read control circuit which compares an input address with the dummy data of an address space of the dummy data storing area, to enable reading of the first application program from the first store when the input address and the dummy address are not identical, and to disable the reading of the first application program and enable the reading of the second application program

from the second store when the input address and the dummy address are identical (Figure 1 item 21A, column 2 lines 31 – 42, column 5 lines 3 – 21).

Takata does not explicitly disclose the presence of a dummy data in a first storing region. Takata describes the presence of defective data in the first storing area (column 3 lines 45 – 63). The defective data is analogous to the dummy data delineated in the application in that both kinds of data do not serve contain information necessary for the proper utilization of the data block, and both data types need to be replaced with useful data. The defective data is replaced with modification data, which is analogous to the dummy data being replaced with regular data. Both functions result in the completion of a data block by replacing one non-regular data with the regular data. Therefore it would have been obvious at the time the applicant's invention was made to use dummy data instead of the defective data because both are same in function and both are replaced with a regular data to complete the data block. This replacement of the defective or dummy data would provide a benefit in adding or modifying of an "unwritable memory device used in game machines, mobile terminals, and the like" (column 1 lines 5 – 10).

Regarding claim 9, Takata discloses:

A memory device for a game machine storing a game program and having a security function for preventing unauthorized use of the game program, comprising:

a first store including a first program storing area for fixedly storing a first portion of the game program and a dummy data storing area for fixedly storing dummy data in place of a second portion of the game program, the second portion being necessary for use of the game program (column 3 lines 45 – 63);

a second store including a second program storing area which has a storage capacity equal to at least a storage capacity of the dummy data storing area of the first stores the second portion of the game program (Figure 1 item 21B, column 3 lines 40 – 63); and

a read control circuit which compares an input address with a dummy address corresponding to an address space of the dummy data storing area and which enables reading of the first portion of the game program from the first store when the input address and the dummy address do not correspond, and disables the reading of the first portion of the game program and enables the reading of the second portion of the game program from the second store when the input address and the dummy address correspond (Figure 1 item 21A, column 2 lines 31 – 42, column 5 lines 3 – 21).

Takata does not explicitly disclose the presence of a dummy data in a first storing region. Takata describes the presence of defective data in the first storing area (column 3 lines 45 – 63). The defective data is analogous to the dummy data delineated in the application in that both kinds of data do not serve contain information necessary for the proper utilization of the data block, and both data types need to be replaced with useful data. The defective data is replaced with modification data, which is analogous to the dummy data being

replaced with regular data. Both functions result in the completion of a data block by replacing one non-regular data with the regular data. Therefore it would have been obvious at the time the applicant's invention was made to use dummy data instead of the defective data because both are same in function and both are replaced with a regular data to complete the data block. This replacement of the defective or dummy data would provide a benefit in adding or modifying of a "unwritable memory device used in game machines, mobile terminals, and the like" (column 1 lines 5 – 10).

Regarding claim 14, Takata discloses:

A method of preventing unauthorized use of regular data stored in a storage device comprising:

storing in a first storage area a first portion of the regular data and storing dummy data in a dummy data area of said first storage area in place of a second portion of the regular data, the second portion of the regular data being necessary for use of the regular data(column 3 lines 45 – 63);

storing in a second storage area having a storage capacity equal to at least a storage capacity of the dummy data storing area of the first storage area the second portion of the regular data (Figure 1 item 21B, column 3 lines 40 – 63); and

comparing an input address with a dummy address corresponding to an address space of the dummy data storing area and enabling reading of the first portion of the regular data from the first storage area when the input address and

the dummy address do not correspond and disabling the reading of the first portion of the regular data and enabling the reading of the second portion of the regular data from the second storage area when the input address and the dummy address correspond (Figure 1 item 21A, column 2 lines 31 – 42, column 5 lines 3 – 21).

Takata does not explicitly disclose the presence of a dummy data in a first storing region. Takata describes the presence of defective data in the first storing area (column 3 lines 45 – 63). The defective data is analogous to the dummy data delineated in the application in that both kinds of data do not serve contain information necessary for the proper utilization of the data block, and both data types need to be replaced with useful data. The defective data is replaced with modification data, which is analogous to the dummy data being replaced with regular data. Both functions result in the completion of a data block by replacing one non-regular data with the regular data. Therefore it would have been obvious at the time the applicant's invention was made to use dummy data instead of the defective data because both are same in function and both are replaced with a regular data to complete the data block. This replacement of the defective or dummy data would provide a benefit in adding or modifying of a "unwritable memory device used in game machines, mobile terminals, and the like" (column 1 lines 5 – 10).

Clam 2 is rejected as applied above in rejecting claim 1. Furthermore, Takata discloses:

A semiconductor storage device according to claim 1, wherein the first store includes a masked ROM, and the second store includes a nonvolatile semiconductor memory which is a writable/readable memory (column 3 lines 32 – 39).

Claim 5 is rejected as applied above in rejecting claim 1. Furthermore, Takata discloses:

A semiconductor storage device according to claim 1, wherein the read control circuit includes a comparator for comparing the input address and the dummy address with each other to output a first signal or a second signal, an enabling/disabling circuit for enabling the first store in response to the first signal and disabling the first store in response to the second signal, and a read address output circuit for outputting a read address for the second portion of the regular data stored in the second store in response to the second signal (Figure 2 item 3, column 4 lines 20 – 55).

Claim 10 is rejected as applied above in rejecting claim 9. Furthermore, Takata discloses:

A memory device according to claim 9, wherein the first store includes a masked ROM, and the second store includes a nonvolatile semiconductor memory which is a writable/readable memory (column 3 lines 32 – 39).

Claim 13 is rejected as applied above in rejecting claim 9. Furthermore, Takata discloses:

A memory device according to claim 9, wherein the read control circuit includes a comparator for comparing the input address and the dummy address with each other to output a first signal or a second signal, an enabling/disabling circuit for enabling the first store in response to the first signal and disabling the first store in response to the second signal, and a read address output circuit for outputting a read address for the second portion of the regular data being stored in the second store in response to the second signal (Figure 2 item 3, column 4 lines 20 – 55).

Claim 15 is rejected as applied above in rejecting claim 14. Furthermore, Takata discloses:

A method according to claim 14, wherein the first storage area resides in a masked ROM, and the second storage area resides in a nonvolatile semiconductor memory which is a writable/readable memory (column 3 lines 32 – 39).

Claim 3 is rejected as applied above in rejecting claim 2. Furthermore, Takata discloses:

A semiconductor storage device according to claim 2, wherein the nonvolatile semiconductor memory has a storage capacity larger than the storage capacity of the second regular data storing area, and further includes a

dummy address storing area other than the second storing area, for storing the dummy address and the dummy address supplied to the read control circuit is read from the dummy address storing area (column 5 lines 1 – 24).

Claim 6 is rejecting as applied above in rejecting claim 2. Furthermore, Takata discloses:

A semiconductor storage device according to claim 2, wherein the nonvolatile semiconductor memory and the read control circuit are formed within the same single memory chip (column 2 lines 22 – 30).

Claim 11 is rejected as applied above in rejecting claim 10. Furthermore, Takata discloses:

A memory device according to claim 10, wherein the nonvolatile semiconductor memory has a storage capacity larger than the storage capacity of the second storing area, and further includes a dummy address storing area, other than the second regular data storing area, for storing the dummy address, and the dummy address supplied to the read control circuit is read from the dummy address storing area (column 5 lines 1 – 24).

Claim 16 is rejected as applied above in rejecting claim 15. Furthermore, Takata discloses:

A method according to claim 15, wherein the nonvolatile semiconductor memory has a storage capacity larger than a storage capacity of the second

storing area, and the method further includes storing a dummy address in a dummy address storing area, and reading the dummy address from the dummy address storage area (column 5 lines 1 – 24).

Claim 17 is rejected as applied above in rejecting claim 15. Furthermore, Takata discloses:

A method according to claim 15, further including writing to the nonvolatile semiconductor memory with a first write voltage in certain areas thereof, and writing with a second write voltage lower than the first write voltage in other areas thereof (column 5 lines 1 – 13, column 7 lines 47 – 51).

Claim 18 is rejected as applied above in rejecting claim 15. Furthermore, Takata discloses:

A method according to claim 15, further including comparing the input address and the dummy address with each other to output a first signal or a second signal, and enabling the first storage area in response to the first signal and disabling the first storage area in response to the second signal, and outputting a read address for the second portion of the regular data being stored in the second storage area in response to the second signal (Figure 2 item 3, column 4 lines 20 – 55).

Claim 4 is rejected as applied above in rejecting claim 3. Furthermore, Takata discloses:

A semiconductor storage device according to claim 3, wherein the nonvolatile semiconductor memory is constructed such that the data is written with a first write voltage in the second regular data storing area and the dummy address storing area, and the data is written with a second write voltage lower than the first write voltage in other areas (column 5 lines 1 – 13, column 7 lines 47 – 51).

Claim 12 is rejected as applied above in rejecting claim 11. Furthermore, Takata discloses:

A memory device according to claim 11, wherein the nonvolatile semiconductor memory is constructed such that the data is written in the second game program storing area and the dummy address storing area with a first write voltage and data is written with a second write voltage lower than the first write voltage into other areas, and in the storing area into which the data is written with the second write voltage, backup data representing a development of the game obtained by executing the game program by a processor of a game machine is written (column 5 lines 1 – 13, column 7 lines 47 – 51).

5. Claims 19 – 27 are storage device claims analogous to the storage device claims rejected above, and therefore, are rejected following the same reasoning.

6. Claims 28 – 32 are method claims analogous to the storage device claims rejected above, and therefore, are rejected following the same reasoning.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaveh Abrishamkar whose telephone number is 571-272-3786. The examiner can normally be reached on Monday thru Friday 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on 571-272-3795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KA
02/02/05

GILBERTO BARRON JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100